

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	6	"5423029" and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and DMA and (ram rom memory storage)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/30 20:06
S2	1	"5423029" and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and DMA and (ram rom memory storage) and test and module	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/05 14:30
S4	5160	(microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/08 09:30
S5	344	direct adj2 tv	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/08 09:31
S6	195	(direct adj2 tv) and satellite	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/08 09:32
S7	30	(direct adj2 tv) and satellite and internet and account and record	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/08 09:43

S8	3	(direct adj2 tv) and satellite and internet and account and record and telemetry	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/08 09:33
S9	1850101	(direct adj2 tv) and satellite and internet and account and record and malfunction near\$4 (satellite spacecraft)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/08 09:48
S10	11	"5940739"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/08 09:51
S11	9211547	"10"/ "023892"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/08 09:51
S12	4	"10023892"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/08 09:52
S13	2	"20020095270"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/08 09:52
S14	1	"5423029" and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/09 16:13
S15	4	("5423029" "5446741" "6480982" "5668815") and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/10 16:28

S16	1	("5423029" "5446741" "6480982" "5668815") and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module and slot	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/10 14:38
S17	2322	(microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module and slot	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/10 14:38
S18	7	"324"/\$.ccis. and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module and slot	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/10 14:42
S19	44	"702"/\$.ccis. and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module and slot	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/10 15:10

S20	8	"73"/\$.ccls. and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module and slot	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/10 14:42
S21	37	"702"/\$.ccls. and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) near4 (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module and slot	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/10 15:13
S22	27	"702"/\$.ccls. and (microprocessor processor controller microcontroller CPU computer microcomputer) and (I/O or (input near2 output)) and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and (test near3 (module slot card))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/10 15:15
S23	52	714/9,42,702,718.ccls. and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/10 16:28

S24	12	714/9.cds. and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/10 16:32
S25	2	714/9.cds. and (microprocessor processor controller microcontroller CPU computer microcomputer) and (input near2 output) and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test near2 (card module)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/23 18:09
S26	120	"714"/\$.cds. and (microprocessor processor controller microcontroller CPU computer microcomputer) and (input near2 output) and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test near2 (card module)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/10 16:41
S27	91	"714"/\$.cds. and (microprocessor processor controller microcontroller CPU computer microcomputer) and (input near2 output) and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test adj2 (card module)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/10 17:16

S28	8	"714"/\$.cds. and (microprocessor processor controller microcontroller CPU computer microcomputer) and (input near2 output) and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test adj2 (card module) and expansion near2 slot	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/11 17:01
S29	26	(microprocessor processor controller microcontroller CPU computer microcomputer) and (input near2 output) and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test adj2 (card module) and expansion near2 slot and (operating adj2 system)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/11 17:06
S30	0	(microprocessor processor controller microcontroller CPU computer microcomputer) and (input near2 output) and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test adj2 (card module) and expansion near2 slot and (operating adj2 system) and (bus adj2 bridge)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/11 17:07
S31	8	714/9,25.cds. and (microprocessor processor controller microcontroller CPU computer microcomputer) and (input near2 output) and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test near2 (card module)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/25 14:38

S32	1	717/105.ccls. and (microprocessor processor controller microcontroller CPU computer microcomputer) and (input near2 output) and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test near2 (card module) and bus and system and error and slot\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/09 13:33
S39	74	"5396619" "2003065470" "5621886" "5446741" "5619513" "5668815" "20030005373"	USPAT	OR	OFF	2005/08/09 14:14
S40	5	("5396619" "2003065470" "5621886" "5446741" "5619513" "5668815" "20030005373") and I/O same controller same dma	USPAT	OR	OFF	2005/08/09 14:16
S41	6	("5396619" "2003065470" "5621886" "5446741" "5619513" "5668815" "20030005373") and I/O and controller and dma	USPAT	OR	OFF	2005/08/09 14:16
S42	3	("5396619" "2003065470" "5621886" "5446741" "5619513" "5668815" "20030005373") and I/O and controller and dma and test	USPAT	OR	OFF	2005/08/09 14:16
S43	2	("5396619" "2003065470" "5621886" "5446741" "5619513" "5668815" "20030005373") and I/O and controller and dma and test same (module card device)	USPAT	OR	OFF	2005/08/09 14:17
S44	3	("5396619" "2003065470" "5621886" "5446741" "5619513" "5668815" "20030005373") and I/O and controller and dma and test same (module card device)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/10 10:34

S45	3	("5396619" "2003065470" "5621886" "5446741" "5619513" "5668815" "20030005373" "5621883" "2214671" "2268295" 98/07163) and I/O and controller and dma and test same (module card device)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/10 10:40
S46	2	"20030005373".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/10 10:40
S47	4	"20030005373".pn. "56199513".pn. "5668815". pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/10 10:50
S48	0	(DMA (direct adj memory adj access)) same (expansion near5 slot)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/10 10:51
S49	108	(DMA (direct adj memory adj access)) same (expansion near5 slot)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/10 10:52
S50	3	(DMA (direct adj memory adj access)) same (expansion near5 slot) with test	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/10 10:54
S51	5	(DMA (direct adj memory adj access)) same (expansion same slot) with test	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/10 11:01
S52	7	(DMA (direct adj memory adj access)) same (ISA, EISA, VESA, PCI, AGP, AMR,CNR slot) same test \$4 near4 card\$2 and test \$5 near6 (memory ram rom storage)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/10 11:06
S53	7	(DMA (direct adj memory adj access)) same (ISA, EISA, VESA, PCI, AGP, AMR,CNR slot) same test \$4 near4 card\$2 and test \$5 near6 (memory ram rom storage cache)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/10 12:38

S54	39	(DMA (direct adj memory adj access)) and (ISA, EISA, VESA, PCI, AGP, AMR,CNR slot) same test \$4 near4 card\$2 and test \$5 near6 (memory ram rom storage cache)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/10 12:38
S55	35	(DMA (direct adj memory adj access)) and (ISA, EISA, VESA, PCI, AGP, AMR,CNR slot) same test \$4 near4 card\$2 and test \$5 near4 (memory ram rom storage cache)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/10 14:09
S56	9	"714"/\$.cccls. and (DMA (direct adj memory adj access)) and (ISA, EISA, VESA, PCI, AGP, AMR,CNR slot) same test\$4 near4 card\$2 and test\$5 near4 (memory ram rom storage cache)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/10 16:04
S57	76	"714"/\$.cccls. and (DMA (direct adj memory adj access)) with test\$5 near4 (memory ram rom storage cache)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/10 16:04
S58	5	test near4 (module card) same (direct adj memory adj access dma) same portion	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/07 18:18
S59	5	test near4 (module card) same (direct adj memory adj access dma) same portion	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/07 18:27
S60	41	"2268295" "5621883" "5446741" "5619513" "2214671" 98/07163	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/07 18:28
S61	0	S60 and test near4 (module card) same (direct adj memory adj access dma) same portion	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/07 18:28
S62	0	S60 and test\$4 near4 (module card) same (direct adj memory adj access dma)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/07 18:28

S63	4	S60 and test\$4 near4 (module card)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/07 18:36
S64	61	test\$4 near3 (module card) same memory same dma	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/07 21:38
S65	6	test\$4 near3 (module card) same memory same dma same portion	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/07 19:18
S66	45	test\$4 near3 (module card) same memory same dma and test\$4 near4 memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/07 21:39
S67	61	test\$4 near3 (module card) same memory same dma sametest\$4 near4 memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/07 21:39
S68	29	test\$4 near3 (module card) same memory same dma same test\$4 near4 memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/07 21:39
S69	11	test\$4 near3 (card) same memory same dma same test\$4 near4 memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/08 11:54
S70	2	"5311426".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/08 11:54
S71	4	"4315330".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/15 11:19
S72	409	test with card and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and (output i/o) and DMA and (ram rom memory storage)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/28 22:51

S73	51	test with card and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and (output i/o) and DMA and (ram rom memory storage) and expansion with slot	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/28 22:52
S74	51	test with card and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and (output i/o) and DMA and (ram rom memory storage) and expansion with slot and test\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/28 23:02
S75	51	test with card and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and (output i/o) and (DMA direct adj memory adj access) and (ram rom memory storage) and expansion with slot and test\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/28 23:03
S76	28	test with card and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and (output i/o) and (DMA direct adj memory adj access) and (ram rom memory storage) and expansion with slot and test\$4 and (part portion) with memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/28 23:30
S77	8	test with card and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and (output i/o) and (DMA direct adj memory adj access) and (ram rom memory storage) and expansion with slot and test\$4 and access with (part portion) with memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/28 23:16

S78	2	"5381541".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/28 23:16
S79	1	test with card and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and (output i/o) and (DMA direct adj memory adj access) and (ram rom memory storage) and expansion with slot and test\$4 with dma and (part portion) with memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/28 23:31
S80	1	test with card and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and (output i/o) and (DMA direct adj memory adj access) and (ram rom memory storage) and expansion with slot and test\$4 with dma with (part portion) with memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/28 23:31
S81	1	test with card and test\$4 with dma with (part portion) with memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/28 23:32
S82	26473	(microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and DMA and (ram rom memory storage)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/30 11:14
S83	124	(microprocessor processor controller microcontroller CPU computer microcomputer) and dma same test\$4 same portion same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/30 11:20
S84	93	(microprocessor processor controller microcontroller CPU computer microcomputer) same dma same test\$4 same portion same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/30 11:21

S85	4	(microprocessor processor controller microcontroller CPU computer microcomputer) same dma same test\$4 with card same portion same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/30 11:21
S86	4	(microprocessor processor controller microcontroller CPU computer microcomputer) same dma same test\$4 with (slot card) same portion same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/30 11:21
S87	9	(microprocessor processor controller microcontroller CPU computer microcomputer) same dma same test\$4 same portion same memory and test with card	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/30 11:22
S89	9	(microprocessor processor controller microcontroller CPU computer microcomputer) same input with output same DMA same (ram rom memory storage) same test with card	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/30 20:33
S90	11	("5621883" "5446741" "5619513" "2214671" 98/07163 "2268295") and dma	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/30 20:36
S91	1	("5621883" "5446741" "5619513" "2214671" 98/07163 "2268295") and dma and test\$4 with card	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/30 20:34
S92	72	710/22.ccls. and dma and test and card	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/30 20:37
S93	26	710/22.ccls. and dma and test with memory and card	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/30 20:39
S94	2	710/22.ccls. and dma and test\$4 with memory and card near4 test	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/30 21:37

S95	4	"2003022962"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/30 21:38
S96	0	"2003/022962"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/30 21:38
S97	1	10/750342	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/30 21:50
S98	0	"2000115385"	USPAT	OR	OFF	2008/07/08 12:57
S99	0	"2000115385"	US-PGPUB; USPAT	OR	OFF	2008/07/08 13:00
S100	0	"2001015385"	US-PGPUB; USPAT	OR	OFF	2008/07/08 13:03
S101	1	"20030115385"	US-PGPUB; USPAT	OR	OFF	2008/07/08 13:04

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	24	(702/186).OCLS	UPAD	OR	OFF	2010/05/27 12:32
L2	651	702/186.ccls.	USPAT; UPAD	OR	ON	2010/05/27 12:32
L3	336	702/186.ccls. and memory and test\$4	USPAT; UPAD	OR	ON	2010/05/27 12:33
L4	535	702/186.ccls. and memory sametest\$4	USPAT; UPAD	OR	ON	2010/05/27 12:33
L5	163	702/186.ccls. and memory same test\$4	USPAT; UPAD	OR	ON	2010/05/27 12:33

5/ 27/ 2010 12:33:45 PM

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